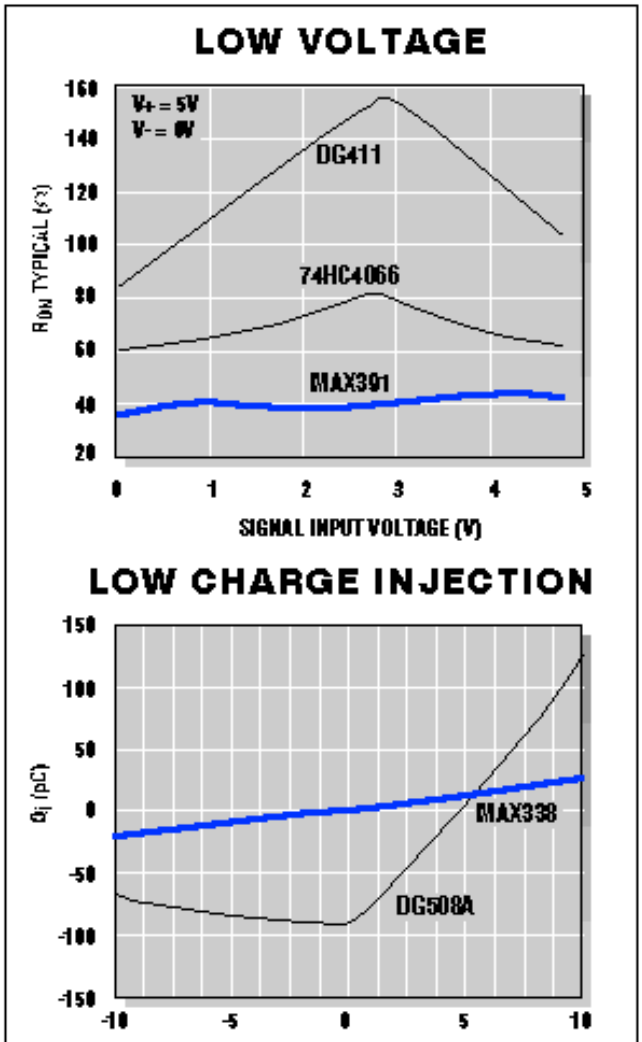
Maxim's Analog Switches and Multiplexers Lead the Industry in Low Voltage, Low Leakage, and High Performance

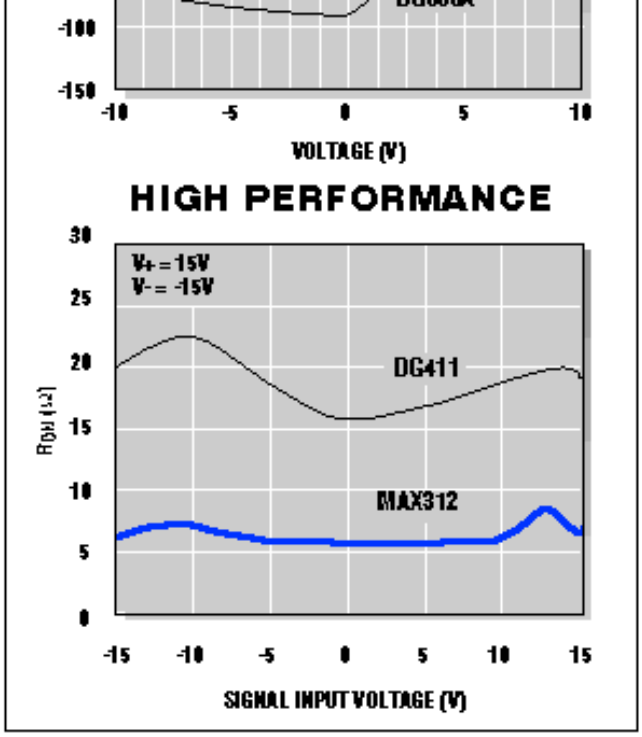
Discusses the advantages of using an analog switch in analog design. Provides simplified modeling of an analog switch and key characteristics. Discusses how these characteristics impact specific applications.

Maxim offers an entire range of analog switches for numerous types of applications including low-power, low-voltage, and/or high-performance systems.

For more than twenty-five years, monolithic analog switches and multiplexers have served as fundamental building blocks in analog circuit design. Integrated-circuit switches have replaced most signal-switching circuits made from discrete component transistors and logic-level shifters. Equally important, IC switches have continued to benefit from process and design improvements that reduce supply voltage, power consumption, on-resistance, charge injection, and switching time.

Switch and multiplexer architectures have not changed in many years, but the constant demand for lower supply voltage, better precision, and tighter spec tolerance obliges manufacturers to persevere with development-if only to achieve incremental performance improvements. To appreciate what the latest switch and multiplexer products can do, consider the components integrated on a typical chip.





Circuit blocks

For most of today's analog switches, the actual switching element is a pair of metal-oxide-semiconductor field-effect transistors (MOSFETs). Unlike bipolar transistors, MOSFETs can handle bidirectional drain-to-source channel currents. Moreover, a voltage-controlled MOSFET is free of the error caused by base-to-emitter currents in a bipolar transistor. MOSFET switches exhibit on-resistance, but no dc offset.

In switching applications, enhancement-mode MOSFETs-offering better characteristics and easier fabrication-are preferable to depletion types. Enhancement-mode types are self-isolating, with drain and source regions formed in a single diffusion step. Because all active regions are reverse-biased with respect to each other and the substrate, adjacent devices on the same substrate are electrically isolated without recourse to dielectric isolation or other special techniques. The MOSFET's insulated gate minimizes the effect of dc control voltage on the signal channel.

A single n-channel or p-channel enhancement-mode MOSFET can serve as an analog switch, but its on-resistance will vary considerably with signal voltage. Connecting an n-channel and p-channel device in parallel-the almost universal configuration for CMOS analog switches-greatly reduces this variation. Complementary gate-drive signals turn the two devices on or off simultaneously. **Figure 1** shows the cross section of an n-channel and p-channel device as they appear in a monolithic structure.

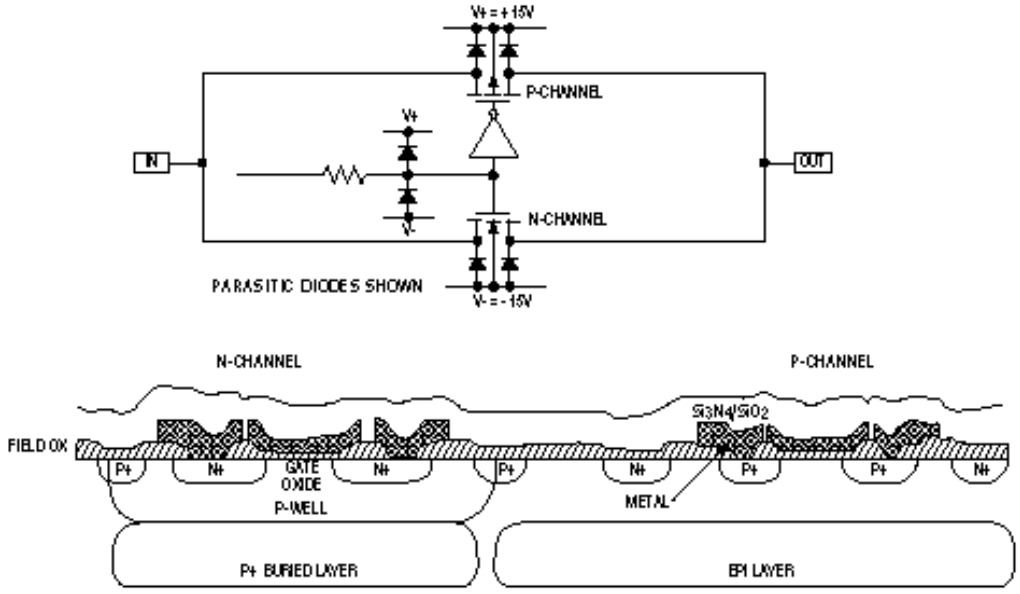


Figure 1. This cross section of the two MOSFETs in an IC transmission gate shows parasitic diodes tied to the supply rails.

The need for fault-tolerant switching has brought about a major exception to the parallel-FET arrangement. By connecting an n-channel, a p-channel, and an n-channel device in series, you can implement a switch channel that turns off automatically when the analog signal approaches either power rail (see *Selection Guides-Fault Protection*).

On-resistance characteristics are the key to understanding these major switch architectures. On-resistance in either device type alone (p or n) is a strong function of the gate-source bias. But connecting the devices in parallel yields an on-resistance that is relatively constant for most of the analog-signal range (**Figure 2**). Processing improvements have repeatedly lowered the gate-source threshold, from that of metal-gate technology (2.5V to 5V) to that of silicon-gate technology (about 900mV).

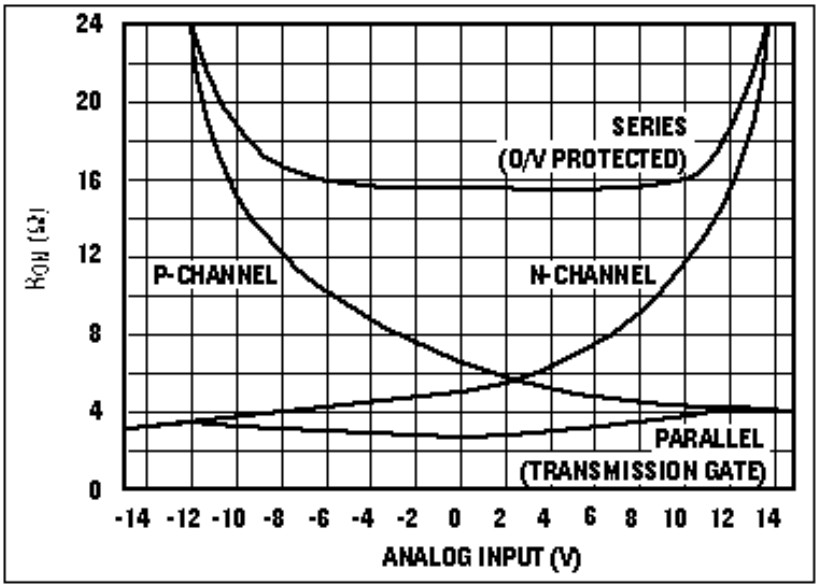


Figure 2. The on-resistance of an n-channel or p-channel MOSFET by itself is quite large at one extreme of the VIN range, but in parallel, their composite resistance remains relatively flat. RON for an overvoltage-protected switch is

approximately six-times higher because the switching element has three MOSFETs in series.

Adding level translators and complementary gate-drive signals lets you control the switch with an applied logic level (**Figure 3**). Applied to one input of the comparator Q2/Q3, this external level establishes an internal logic state (high or low) with respect to a reference voltage connected to the comparator's other input. The comparator outputs then drive complementary inverting buffers (Q5-Q8) that provide the phase and current gain necessary to charge and discharge gate capacitance in the switching MOSFETs Q9 and Q10.

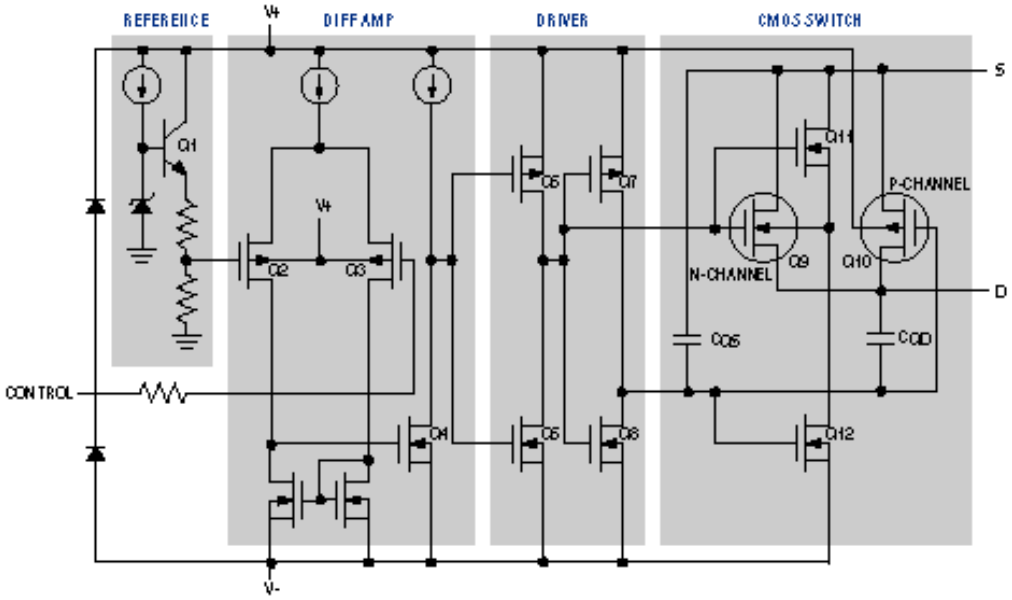


Figure 3. The gate-drive circuitry in this analog switch derives complementary ±15V signals from a single logic level at VIN.

To turn the switch on, connect the n-channel gate to the positive rail and the p-channel gate to the negative rail. One FET is always on as the source connection swings to either extreme of the analog range. The switch can function with its FET body connections tied directly to the supply rails, but the Q11 and Q12 connections shown enhance performance by lowering the switch leakage and reducing the modulation of on-resistance.

Q11 and Q12 form a "body snatcher" for the n-channel switching FET. When the switch is on, Q11 connects the body of Q9 to its source, eliminating modulation of the channel by ensuring a constant source-to-body voltage. When the switch is off, Q12 improves off isolation and leakage by connecting the body of Q9 to the negative rail.

Body-snatcher improvements are not without side effects. If Q11 and Q12 turn on together, even for an instant, they momentarily connect the switch source to the negative rail, producing negative charge injection and lengthening the on/off times. The chip design ensures that these transistors are never on at the same time.

When the switch changes state, the Q5/Q6 and Q7/Q8 inverters produce gate-drive waveforms with sharp edges, which pass through the Q9/Q10 gate-source and gate-drain capacitances and into the analog signal channel. If left uncorrected, the resulting charge-injection spikes can overload downstream circuitry, lengthen settling times, and produce annoying "splats" in an audio loudspeaker. Capacitors C_{QS} and C_{QD} enhance performance by compensating for this charge injection at the source and drain connections.

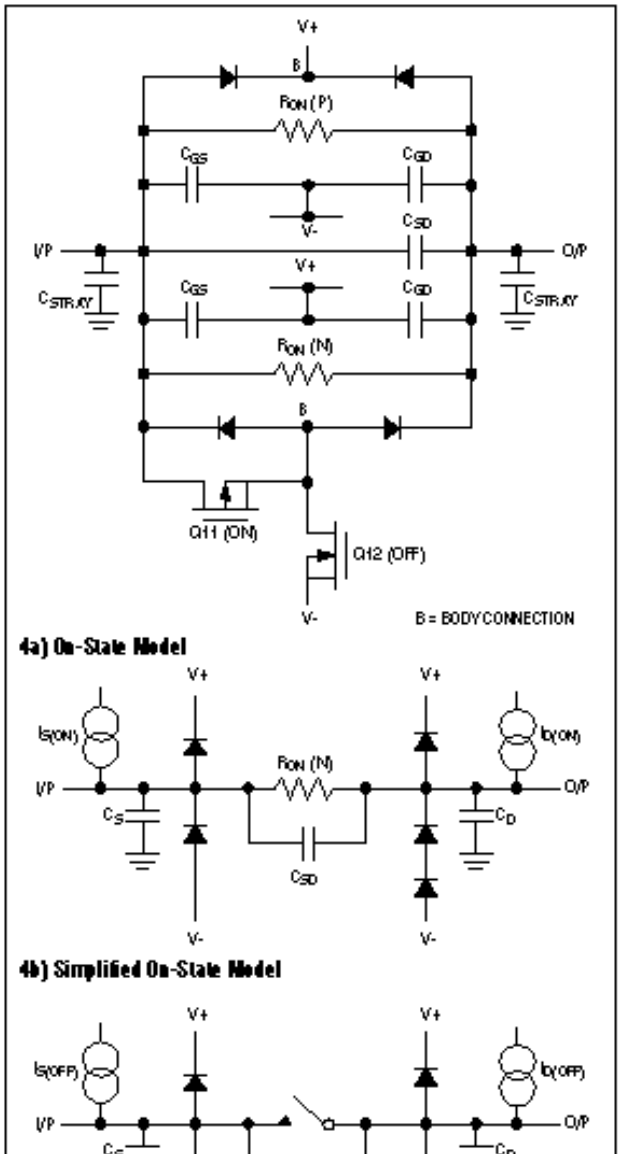
If the gate-source capacitances for equivalent n- and p-channel devices were equal, the IC designer might cancel charge-injection effects by ensuring truly complementary waveforms at the gates of Q9 and Q10. But these capacitances are not equal: the conductance of n-type material is 2.5 to 2.8 times larger than that of p-type material. For equal on-resistances, therefore, the p-channel's size and gate-source capacitance must be 2.5 to 2.8 times larger than that of the n-channel device.

Thus, capacitors C_{QS} and C_{QD} compensate for the geometric imbalance between Q9 and Q10. Each capacitor is a binary-weighted array, trimmed at the mask level for a particular signal voltage (usually 0V in a dual-rail circuit) to minimize charge injection at the source and drain terminals. The complication is that the gate-source and gate-drain capacitances (which are produced by reverse-biased diode junctions) vary with the signal voltage. This effect requires additional, dynamic compensation in the form of extra diodes or a dummy switch.

On-switch (static) modeling

Successful design with analog switches and multiplexers calls for an understanding of parasitic and non-ideal characteristics in the basic switch architecture. Models for the on and off states of a switch let you study its static and dynamic effects on a system. Static (steady-state) effects include on and off capacitances, voltage-swing limits, leakage current, transmission loss, bandwidth, and crosstalk. Dynamic effects include on and off switching times, settling time, and propagation delay.

For the steady-state on condition, the Figure 3 switch can be modeled as in **Figure 4a** and simplified as in **Figure 4b**. First, the power-supply limits determine the analog signal range. If a signal excursion exceeds either power rail, the associated parasitic diode will conduct and inject current into the substrate, producing problems such as gross output distortion and increased leakage in the adjacent switches.



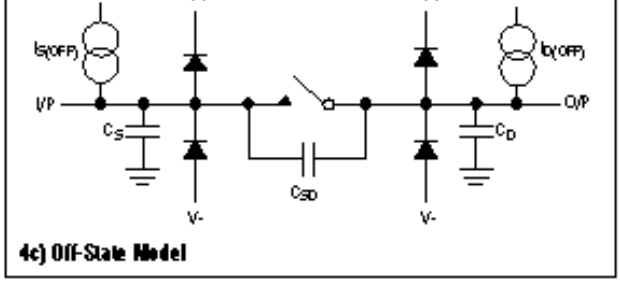


Figure 4. These lumped-parameter models of an analog switch let you estimate the effect of its static and dynamic operation.

At some level of parasitic-diode current, the IC can latch up and destroy itself, so you should limit supply currents per the Absolute Maximum Ratings. On the other hand, if large signals are predictable in your application, consider a fault-tolerant structure such as the series-FET type mentioned earlier, which prevents current flow during overvoltage conditions.

The parasitic diodes in question also cause most of the unwanted leakage specified for an analog switch or multiplexer. In a perfect switch, the diodes would be matched; for equal reverse voltages, the net leakage into and out of the source and drain terminals would be zero. Actual leakages are not matched, of course, so a data sheet must specify the net difference current for each case (see *Selection Guides - Low Leakage*).

To simplify leakage tests during production, manufacturers measure the total on-state leakage at the drain terminal. This current flows through the on-resistance and produces offset-voltage errors, so a high signal-source impedance demands a low switch leakage. Moreover, the analog signal modulates this leakage by varying the reverse bias across the parasitic diodes. To ensure worst-case measurements, the data sheet specifies leakage in the presence of a signal voltage near the supply rails, which subjects the diodes to a maximum imbalance in reverse bias.

For small-signal low-frequency conditions, you can define input-to-output transmission loss (L_{TRANS}, in dB) in terms of on-resistance and the output load resistance R_L:

$$L_{TRANS} = 20\log[R_L / (R_L + R_{ON})].$$

R_{ON} is proportional to absolute temperature, so L_{TRANS} is also a function of temperature. Small signal is defined as small enough to avoid modulation of the on-resistance (100mV or less). Larger signals, up to those encompassing the full dynamic range of the switch, produce a distortion error (D, in percent) due to the change of on-resistance with analog signal swing:

$$D = 100\Delta R_{ON} / R_L.$$

Thus, to achieve lowest distortion when operating in the voltage mode, you must minimize ΔR_{ON} and maximize R_L. The specifications for recent products help you implement this goal: MAX3xx switches and multiplexers, for example, are the first to provide-in addition to static on-resistance-separate specs for channel-to-channel matching and for signal swing vs. dynamic variation about the static value (see *Selection Guides - Low On-Resistance*).

"The lower the better" applies for on-resistance in most applications. An excellent way to produce low-on-resistance switches from standard parts is to parallel the switch sections in a single IC. Using switches from the same die assures a good match in the logic propagation delays. For example, the MAX351 (a precision quad SPST switch) can be wired in parallel to produce an on-resistance of 5.5Ω typical and 11.25Ω maximum, with a corresponding ΔRON of only 1.25Ω maximum. The parallel connection handles more signal current while lowering the distortion and transmission loss, but it also increases the leakage and charge injection.

Another parameter affected by on-resistance is the f-3dB bandwidth. RON and CDRAIN alone determine bandwidth if the switch is driven with a pure voltage source (**Figure 5a**). Otherwise, the non-zero source impedance must be accounted for (**Figure 5b**):

$$f_{-3dB} = 2\pi \frac{R_A - R_{LOAD}}{R_A + R_{ON}},$$

where RA = (RSOURCE + RON).

On-resistance and drain on-capacitance are not lumped parameters; both are distributed along the channel of the switching FET. For calculating actual bandwidths, these quantities are more accurately modeled as multiple sections (**Figure 5c**). This model is suitable for frequencies above 500kHz and for pulse applications in which you must calculate the signal's propagation delay through an on channel.

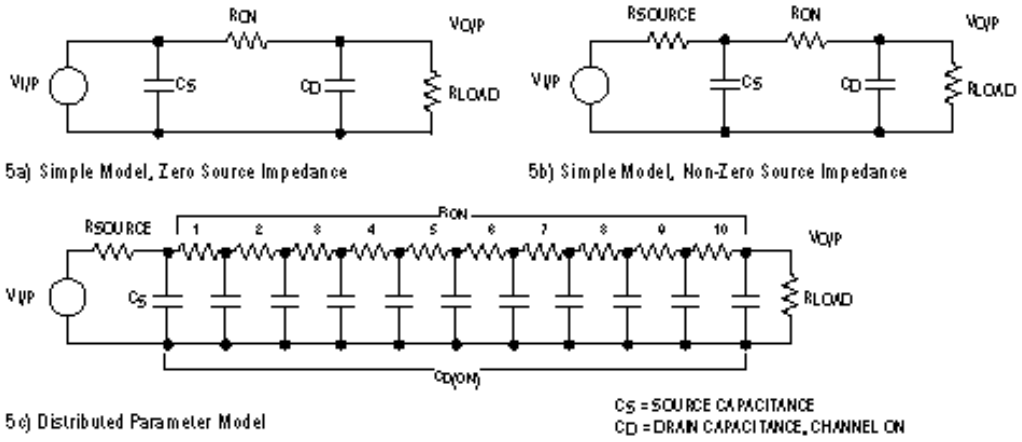


*Figure 5. A simple switch-bandwidth model (**a**) is made more accurate by adding source impedance (**b**), and more accurate still by representing the distributed RON and CD as a cascade of sections (**c**).*

Off-switch (static) modeling

Off isolation and leakage are primary concerns in the off state; other parameters of interest are the signal-voltage limits, the power-supply levels and tolerances, and the input and output logic levels. You can estimate off isolation within the switch using the transmission-loss equation and a suitable switch model (**Figure 4c**). First, include in the equation the impedance effect of the drain-source capacitance, CSD. Isolation depends as much on external layout as device characteristics, so when possible, you should measure its actual value in a circuit.

Off-state leakage (like on-state leakage) originates in parasitic diodes associated with the switching MOSFETs. It can be modulated by analog signals applied to the off channel, which in turn are limited by the power supplies (as for an on channel). Signal voltage beyond either supply rail causes current flow into the substrate, thereby introducing problems that depend on the current's polarity and magnitude.

Maximum supply voltages are determined by the chip's semiconductor process, and minimum values are determined by the process and the internal gate-to-source thresholds required for the switching FETs. Thus, supply rails for the standard-product DG4xx and DG5xx multiplexer families and the DG2xx, DG3xx, and DG4xx switch families may range from ±4.5V to ±22V. The single-rail limit for these products is 30V. Low-voltage, low-RON families such as Maxim's MAX38x and MAX39x specify ±2.7V to ±8V for dual rails and 2.7V to 16V for the single rail (see *Selection Guides - Low Voltage*).

Supply currents are specified in the data sheet, but the analog switch itself draws no current. Comprised of n- and p-channel MOSFETs in parallel, the switch is a passive device that draws no power from the supplies. Instead, supply currents are drawn by the digital interface, which converts applied logic levels to the gate-drive signals required by these parallel MOSFETs. The currents vary with applied voltage level, and they peak when the level translator is operating in its linear mode. This mode, unfortunately, occurs near the TTL levels of 0.8V and 2.4V (**Figure 6**) and produces the worst-case supply currents. If the logic voltages swing rail to rail (as when logic and analog supply voltages are equal), the supply currents drop almost to leakage levels-certainly to below 1µA.

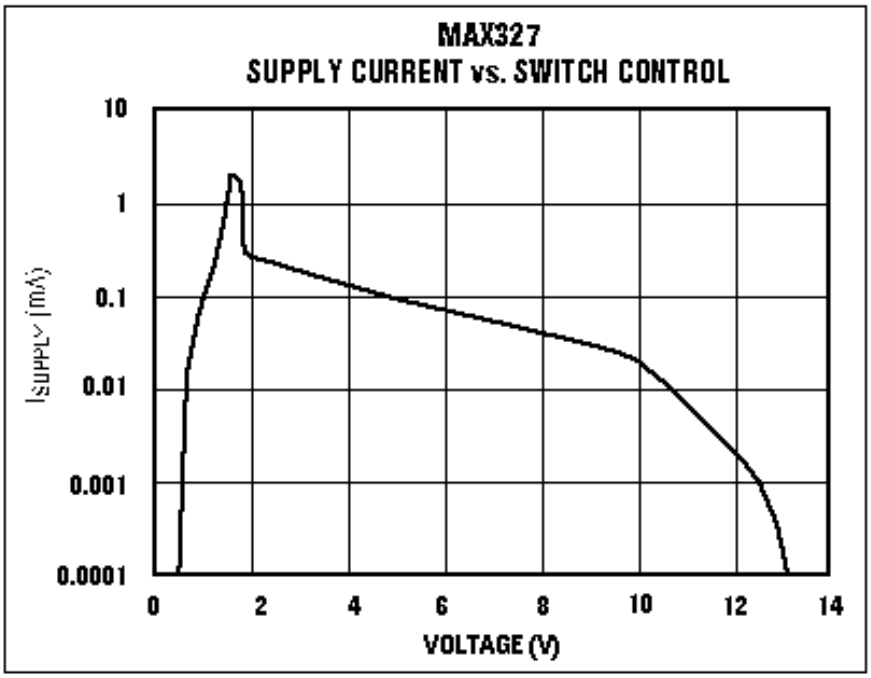


Figure 6. Input current at the VIN control input of an analog switch peaks near the TTL levels of 0.8V and 2.4V.

The saturated logic drivers Q7/Q8 and Q5/Q6 provide low-impedance paths from the supply rails to the analog channel, via the gate-to-channel capacitances in Q9 and Q10. Thus, high-frequency noise can couple from each supply rail to the channel and vice versa, unless you add a decoupling network at each supply terminal. More than adequate for this purpose is 100Ω in series, shunted by 10µF in parallel with 100nF.

Most analog-switch ICs have an individual address line for each switch, up to the maximum number (of switches) practical without decoding the address on chip. This number is about four. The preferred technique for controlling more than four switches on an IC is a serial interface that reduces the pin count and provides individual control.

For example, the MAX335-an array of eight switches in a 24-pin package-clearly illustrates the flexibility of serial control. Some such chips include digital latches with an option for transparent operation, but that arrangement may allow significant crosstalk from the active digital bus to the analog channels. If so, you may have to add an external latch to physically isolate the bus from the switches.

Dynamic switching effects

We've presented electrical models of the analog switch and linked the models to the specifications that describe a switch in the static state-on or off. Next, we consider the specifications associated with dynamic behavior; i.e., switch phenomena that occur during a change of state.

Switching time, for example, is the sum of the propagation delay through the level shifter and the time it takes for

load voltage to rise (or fall) to a predetermined level (**Figure 7**). Propagation delay is generally defined as the time interval from 50% of the logic transition (V_{IN}) to 90% of the output-voltage transition.

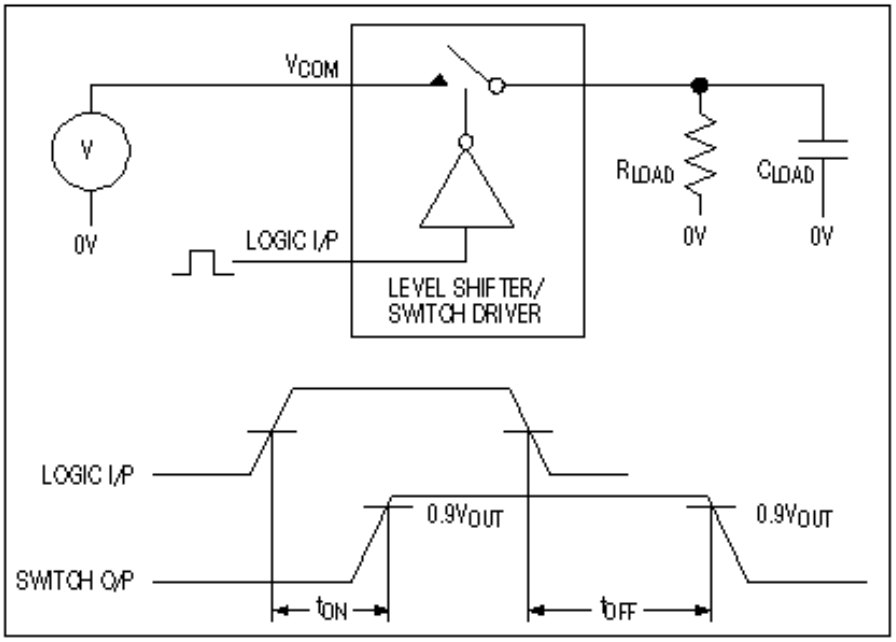


Figure 7. Internal propagation delay and an output time constant determine the on/off times for an analog switch.

Rise and fall times are calculated from load conditions given in the data sheet. Note that manufacturers specify loads with a fast time constant to ensure that the resulting measurements are dominated by the device under test. Thus,

t_{ON} (switch only) = t_{ON} (from the data sheet) - $t_{RISE(load)}$,

where $t_{RISE(load)} = (R_{ON}||R_{LOAD})C_{LOAD}[-\ln(\%\ error/100)]$, and percent error is related to the percent of final value specified in the data sheet. For 90% of the final value (a standard level), the percent error is 10%. Therefore, $t_{RISE(load)} = (R_{ON}||R_{LOAD})C_{LOAD}[-\ln(0.1)] = 2.3(R_{ON}||R_{LOAD})C_{LOAD}$. Similar reasoning applies for switch off time:

t_{OFF} (switch only) = t_{OFF} (from the data sheet) - $t_{FALL(load)}$,

where $t_{FALL(load)} = R_{LOAD}C_{LOAD}[-\ln(\%\ error/100)]$. In this case, the fall time is specified to 10% of the final value, which again leaves 10% as the percent error. Therefore, $t_{FALL(load)} = R_{LOAD}C_{LOAD}[-\ln(0.1)] = 2.3R_{LOAD}C_{LOAD}$.

For multiple switches, the break-before-make interval guarantees (as its name implies) that two inputs cannot be shorted together. MAX338 8-channel multiplexers, for instance, guarantee minimum BBM intervals of 10ns (**Figure 8**).

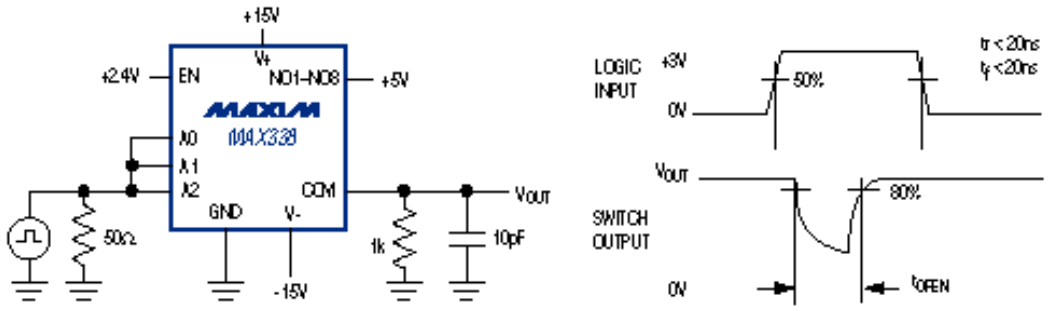


Figure 8. This test configuration enables measurement of the break-before-make interval.

Of all the dynamic specs, settling time is the most problematic to measure. Defined as the time required for VOUT to settle within a specified error band centered on its final value and in response to a change from on to off or off to on, settling time depends on external source and load impedances as well as the switch on-resistance.

A suitable switch model (**Figure 9**) lets you calculate the settling time. For low clocking rates at the address inputs, this model is valid to about 16 bits-a digital resolution comparable to the settling-time perturbations caused by thermal effects on the die. (Neglect of source resistance is a common oversight in these calculations.)

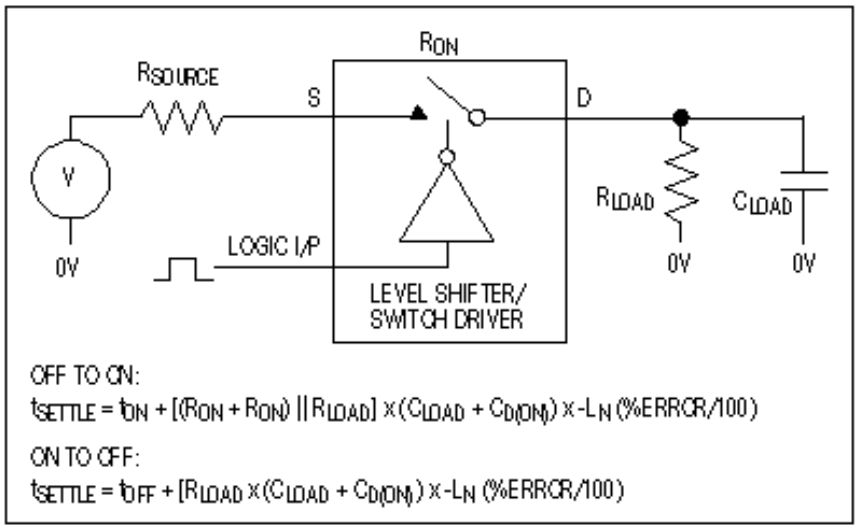


Figure 9. This simple circuit model allows an accurate estimate of settling time.

To support the limits guaranteed for other dynamic specifications, the digital transitions at VIN are necessarily fast. The resulting voltage edges pass through the device capacitances and inject a small charge into the analog channel, which in turn produces a small step of error voltage on the output:

$V_{STEP} = Q / C_{LOAD}$.

If the charge injection (Q) is in picocoulombs and CLOAD is in nano-farads, VSTEP is in millivolts. Comparable amounts of charge are injected at the input and output. In the test setup of **Figure 10**, however, a low source resistance produces almost no voltage error due to charge injection. Voltage error due to output charge injection adds to the settling time. You can calculate that effect as before, noting that the charge-injection step decays to allow

VOUT to settle within the error band. To minimize charge-injection effects, many Maxim ICs require maximum rise and fall times of 20ns at the logic inputs.

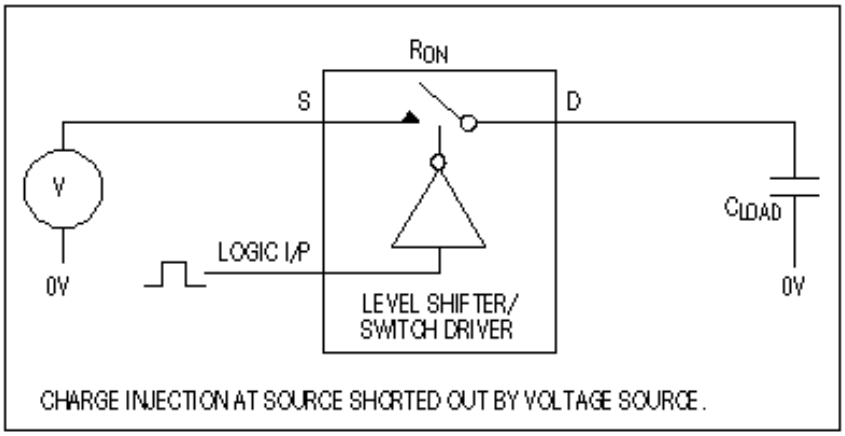


Figure 10. Low signal-source resistance shorts out the effect of charge injection at the source of the switching MOSFET.

Applications

Solid-state switches and multiplexers have many uses beyond the obvious applications in data acquisition and low-frequency signal processing. They can handle RF signals to 1MHz and above, for example, if the switching and isolation requirements permit. Analog switches offer the advantage of low power dissipation and a simple logic interface. Performance depends on signal current in the switching element, which (to reduce transmission loss) is generally limited to a few milliamps.

Two single-supply SPDT switches, for example, let you implement a bandwidth-filter selector for a 455kHz IF signal (**Figure 11**). Low on-resistance, matched sections, and 85dB crosstalk at 1MHz make these switches ideal for RF switching at 1MHz (or less) in portable, battery-powered systems.

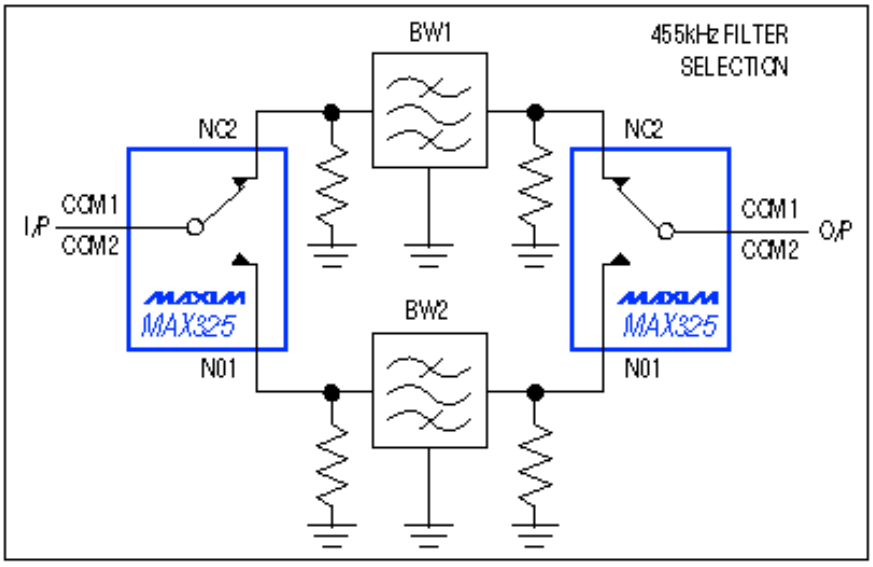
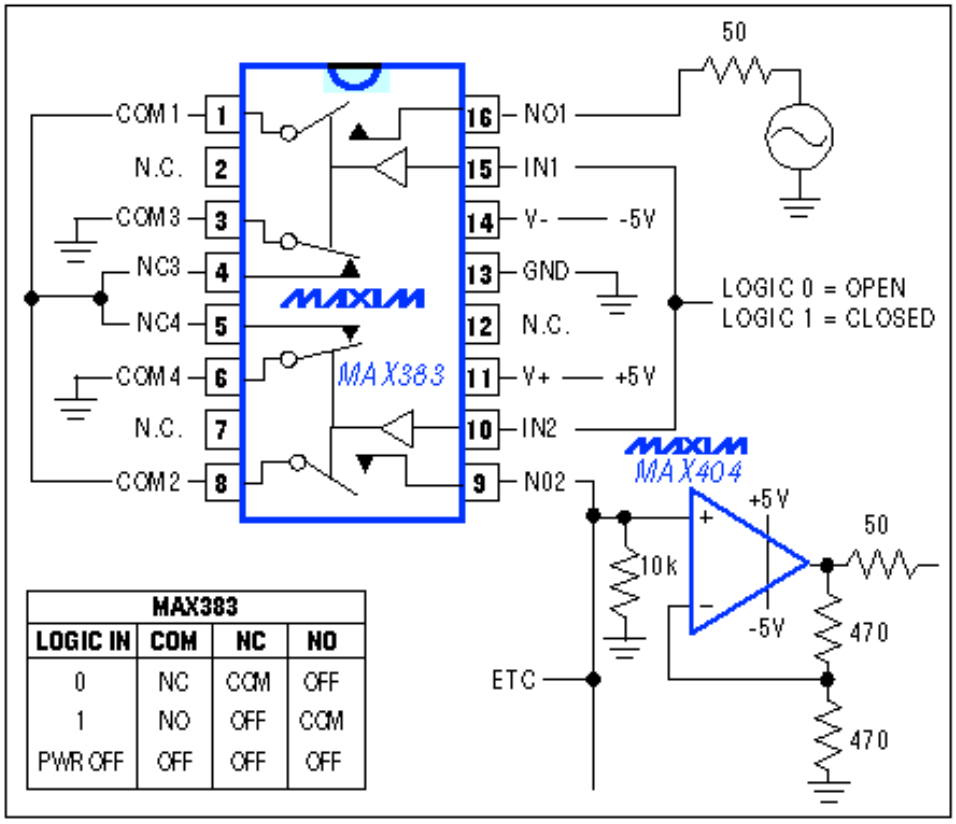


Figure 11. These single-supply SPDT switches handle frequencies as high as 1MHz.

For good crosstalk performance to 10MHz and beyond, consider the buffered T switch connection (**Figure 12**). This IC (the MAX383) can be connected as a single- or dual-rail T switch with low on-resistance (40Ω typical) and excellent off isolation (-80dB at 10MHz). You can add an output buffer to achieve lower distortion and lower transmission loss, but analog switches ultimately fail on crosstalk and isolation as the operating frequency increases.



MAX383			
LOGIC IN	COM	NC	NO
0	NC	COM	OFF
1	NO	OFF	COM
PWR OFF	OFF	OFF	OFF

Figure 12. The buffered T switches in this application provide good performance to 10MHz and beyond.

On the other hand, analog switches have a level-shifting capability that enables them to switch RF signals (**Figure 13**). The applied 5V-logic signal, shifted to ±15V by the switch section, turns the RF switch on or off by biasing or reverse-biasing the two associated diodes. Current levels in the diodes depend upon their type (silicon or PIN) and the specified maximums for transmission loss and intermodulation distortion. Most analog switches can handle about 20mA before encountering their absolute maximum limit.

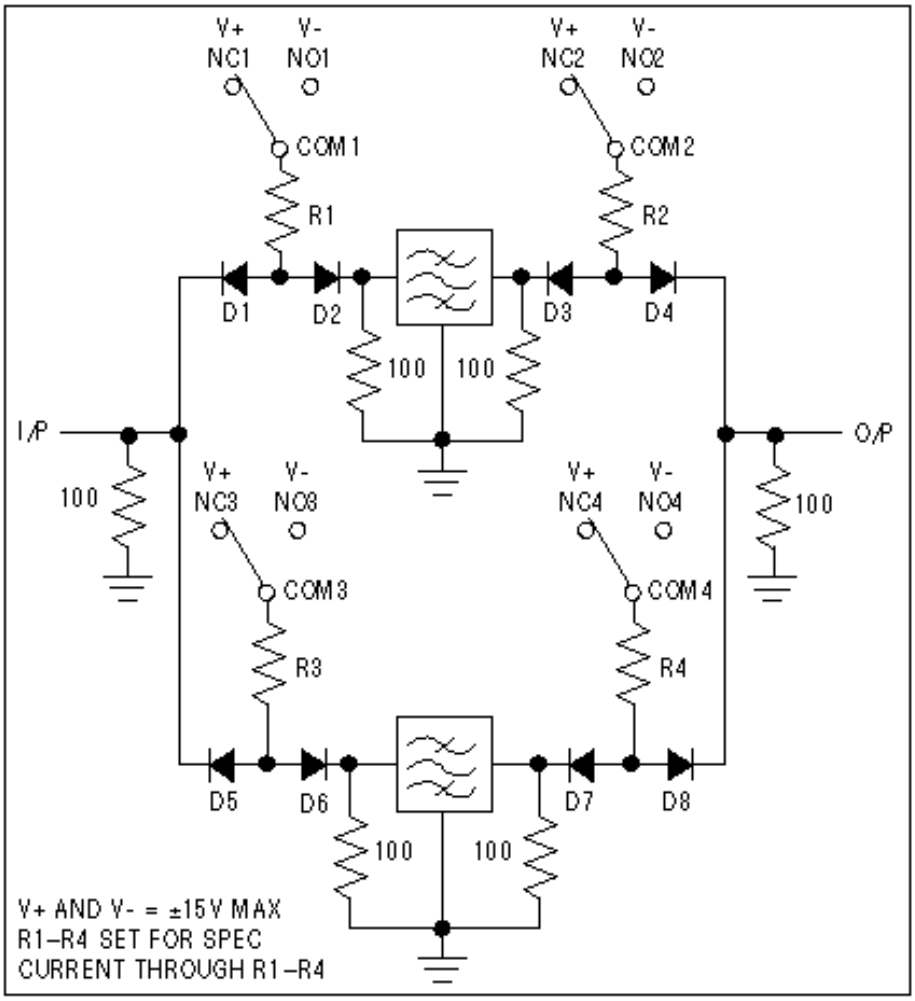


Figure 13. This quad SPDT analog switch (the MAX333A) helps implement four current-controlled RF switches.

To turn the RF switch off, the SPDT switch connects the diodes to -15V. Subject to the diodes' maximum reverse-voltage rating, this configuration ensures good performance and minimum capacitance in the off state. If necessary, you can parallel two sections of the quad-SPST MAX333A to double the current delivered to the diodes.

In another type of current-controlled switch, the switching element consists of an npn- and a pnp-bipolar transistor in parallel (**Figure 14**). The output is a two-collector junction that acts like a current source (in the on state), which enables the designer to make independent choices for the values of gain and output resistance. Output resistance determines the required reverse termination, and in most applications the two resistances together are chosen for unity forward gain through the switch. D1 and D2 protect the base-emitter junctions against excessive reverse voltage in the off state.

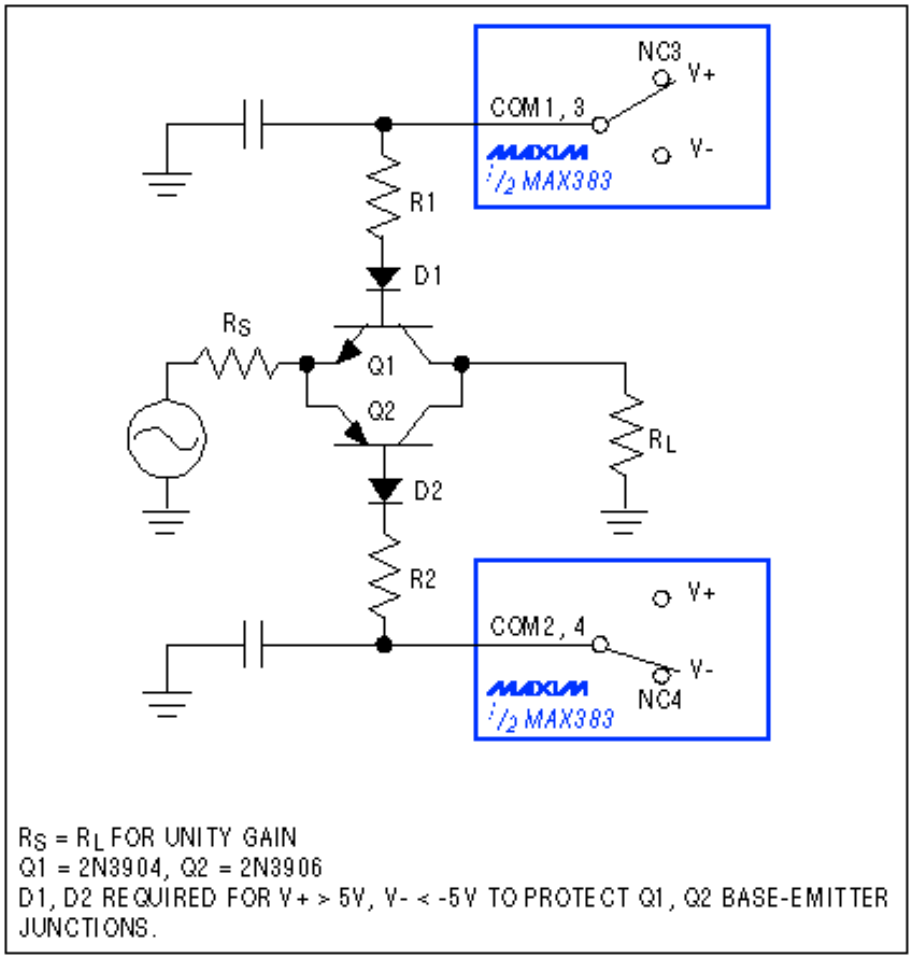


Figure 14. A dual SPDT analog switch (the MAX383) helps implement a current-controlled RF switch consisting of two bipolar transistors in parallel.

Analog switches can also select crystals in a crystal-controlled oscillator (**Figure 15**). As before, the switch either forward-biases or reverse-biases a diode, which in turn selects or deselects the associated crystal. Supply voltages to ±8V can be switched by a MAX383 dual SPDT switch. For higher voltages, to ±18V, use a MAX411 quad SPDT switch.

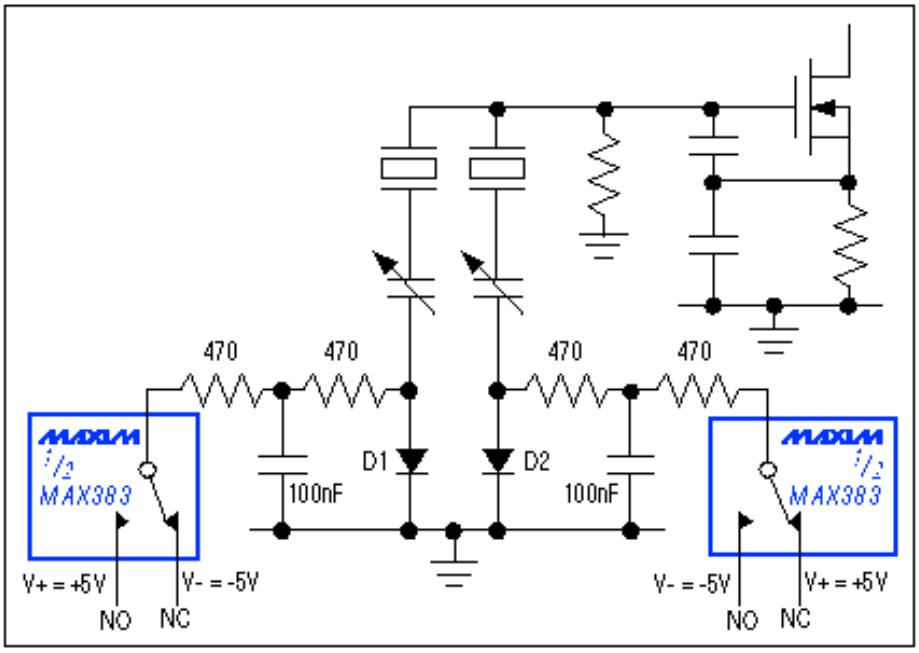


Figure 15. SPDT switches select one of two crystals in this crystal-controlled oscillator.

Signal processing

IC switches and multiplexers are useful in circuits that select discrete levels of gain, frequency, phase, or voltage. Gain-control circuits, for example, can employ either series (**Figure 16a**) or shunt (**Figure 16b**) switching. Each approach offers advantages.

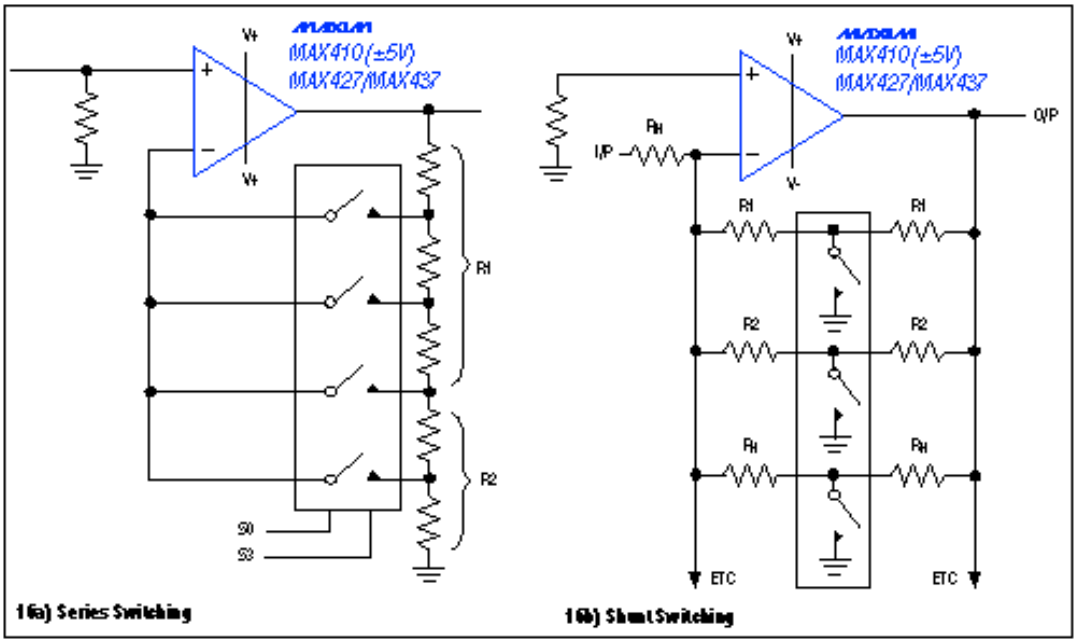


*Figure 16. Gain-control circuits can employ series (**a**) or shunt (**b**) switching.*

For series switching, the signal is not inverted, and the gain is independent of the switch on-resistance. Gain equals

(1 + R1 / R2), where the sum R1 + R2 is constant but the relative values of R1 and R2 depend on which switch is closed. You should keep the sum low to minimize the passband zero caused by C_{STRAY} and R1||R2. A low-leakage switch with low output capacitance also minimizes this effect. You should ensure break-before-make timing to avoid an open-loop condition. Note: by substituting a 16-channel multiplexer such as the MAX306, you can select one of 16 gain levels.

The shunt configuration inverts the signal. It opens all the switches at power-up (to ensure a closed loop with minimum gain) and then closes all switches except the one corresponding to the desired gain. Thus, an open switch associated with R2 (all other switches closed) produces a feedback resistance of 2R2. A closed switch at R_N produces a feedback resistance of $R_N(1 + R_N / R_{ON})$, if $R_{ON} << R_N$. Each pair of resistors isolates a switch capacitance and its effect on bandwidth, but for maximum isolation the R_{ON} value must be low (50Ω or less).

FAULT PROTECTION

Device	Industry Cross	Function (Mux)	Latched Inputs	Fault Protection (V)	Price* ($)
MAX354	ADG508F			±40	2.45
MAX355	ADG509F			±40	2.45
MAX358	DG508A**/HI508A	8:1	–	±35	2.45
MAX359	DG509A**/HI509A	4:2 Diff	–	±35	2.45
MAX368	DG528**/ADG529**	8:1	Yes	±35	3.50
MAX369	DG529**/ADG529**	4:2 Diff	Yes	±35	3.50
MAX378	HI548	8:1	–	±75	3.50
MAX379	HI549	4:2 Diff	–	±75	3.50
MAX388	DG528**	8:1	Yes	±100	4.50
MAX389	DG528**	4:2 Diff	Yes	±100	4.50

* Prices are 1000 pc., FOB USA
** Requires external components for protection

ULTRA-LOW LEAKAGE

Device	Function	Industry Cross	Off Leakage (pA max)	RON (Ω max)	Charge Injection (pC)
MAX326	Quad SPST	DG201	10	2.5k	3 (typ)
MAX327	Quad SPST	DG202	10	2.5k	3 (typ)
MAX328	8-Ch Mux	DG508A	10	2.5k	3 (typ)
MAX329	Dual 4-Ch Mux	DG509A	10	2.5k	3 (typ)
MAX338	8-Ch Mux	DG508A	20	400	5 (max)
MAX339	Dual 4-Ch Mux	DG509A	20	400	5 (max)

LOW ON-RESISTANCE

Device	Function	On-Resistance (Ω max)	R_{ON} Match (Ω max)			R_{ON} Flatness (Ω max)			Charge Injection (pC max)		
			BEST	BETTER	OK	BEST	BETTER	OK	BEST	BETTER	OK
MAX301/DG401	Dual SPST	35	2	2	3	Δ3	Δ3	NT	15	15	NT
MAX303/DG403	Dual SPDT	35	2	2	3	Δ3	Δ3	NT	15	15	NT
MAX305/DG405	Dual DPST	35	2	2	3	Δ3	Δ3	NT	15	15	NT
MAX306/DG406	16-Ch Mux	100	5	10	NT	Δ7	Δ10	NT	10	10	NT
MAX307/DG407	Dual 8-Ch Mux	100	5	10	NT	Δ7	Δ10	NT	10	10	NT
MAX308/DG408	8-Ch Mux	100	5	10	15	Δ7	Δ10	NT	10	10	NT
MAX309/DG409	Dual 4-Ch Mux	100	5	10	15	Δ7	Δ10	NT	10	10	NT
MAX312/DG411	Quad SPST	10	1.5	–	NT	Δ2	–	NT	30	–	NT
MAX313/DG412	Quad SPST	10	1.5	–	NT	Δ2	–	NT	30	–	NT
MAX314/DG413	Quad SPST	10	1.5	–	NT	Δ2	–	NT	30	–	NT
MAX351/DG411	Quad SPST	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
MAX352/DG412	Quad SPST	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
MAX353/DG413	Quad SPST	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
MAX317/DG417	SPST	35	N/A	N/A	NT	Δ3	Δ4	NT	10	10	NT
MAX318/DG418	SPST	35	N/A	N/A	NT	Δ3	Δ4	NT	10	10	NT
MAX319/DG419	SPDT	35	2	3	NT	Δ3	Δ4	NT	10	10	NT
DG421	Dual SPST*	35	N/A	3	NT	N/A	Δ4	NT	N/A	15	NT
DG423	Dual SPDT*	35	N/A	3	NT	N/A	Δ4	NT	N/A	15	NT
DG425	Dual DPST*	35	N/A	3	NT	N/A	Δ4	NT	N/A	15	NT
MAX361/DG441	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT
MAX362/DG442	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT
MAX364/DG444	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT
MAX365/DG445	Quad SPST	85	2	4	NT	Δ5	Δ9	NT	5	10	NT

Best = MAX3xx
Better = Maxim's Improved DG4xx
OK = Competitive Industry Standard

* Latched address inputs
NT = Not Tested

LOW VOLTAGE (2.7V to 16V)

	DEVICE	FUNCTION	ON-RESISTANCE MATCH (Ω max)	ON-RESISTANCE FLATNESS (Ω max)	CHARGE INJECTION (pC max)	PIN COMPATIBLE	µMAX PACKAGE
	SWITCHES						
	MAX320	Dual SPST (NO)	2	6	5	TSCW66F	✔
	MAX321	Dual SPST (NC)	2	6	5	TSCW66F	✔
	MAX322	Dual SPST (NO, NC)	2	6	5	TSCW66F	✔
	MAX323	Dual SPST (NO)	2	6	5	TSCW66F	✔
	MAX324	Dual SPST (NC)	2	6	5	TSCW66F	✔
	MAX325	Dual SPST (NO, NC)	2	6	5	TSCW66F	✔
	MAX381	Dual SPST (NO)	2	6	5	DG401	
	MAX383	Dual SPDT	2	6	5	DG403	
	MAX385	Dual DPST (NO)	2	6	5	DG405	
	MAX391	Quad SPST (NC)	2	6	5	DG411	
	MAX392	Quad SPST (NO)	2	6	5	DG412	
	MAX393	Quad SPST (NO, NC)	2	6	5	DG413	
	MAX394	Quad SPDT	2	6	5	MAX333	
NEW	MAX4066/A	Quad SPST	2	6	10	74HC4066	QSOP
	DEVICE	**FUNCTION**	**ON-RESISTANCE MATCH (Ω max)**	**ON-RESISTANCE FLATNESS (Ω max)**	**CHARGE INJECTION (pC max)**	**PIN COMPATIBLE**	**LATCHED INPUT**
	MUXES						
	MAX382	8-Channel Mux	10	16	5	DG428	✔
	MAX384	Dual 4-Channel Mux	10	16	5	DG429	✔
	MAX395†	8-Channel Mux	10	16	5	MAX335	SERIAL CONTROL
	MAX396	16-Channel Mux	10	16	5	DG406	
	MAX397	Dual 8-Channel Mux	10	16	5	DG407	
NEW	MAX398	8-Channel Mux	10	16	5	DG408	
NEW	MAX399	Dual 4-Channel Mux	10	16	5	DG409	
NEW	MAX4051/A†	8-Channel Mux	15	16	10	74HC4051	
	MAX4052/A†	Dual 4-Channel Mux	15	16	10	74HC4052	
	MAX4053/A†	Triple 2-Channel Mux	15	16	10	74HC4053	

† Future Product—available after November 1995

NEW NEW	MAX399	Dual 4-Channel Mux	10	16	5	DG409	
	MAX4051/A†	8-Channel Mux	15	16	10	74HC4051	
	MAX4052/A†	Dual 4-Channel Mux	15	16	10	74HC4052	
	MAX4053/A†	Triple 2-Channel Mux	15	16	10	74HC4053	

† Future Product—available after November 1995

More Information

MAX325: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX327: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX328: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX383: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX410: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX427: QuickView -- Full (PDF) Data Sheet -- Free Samples

MAX437: QuickView -- Full (PDF) Data Sheet -- Free Samples